REMARKS

Claims 1-20 stand rejected.

Claims 1-3, 8, and 13 are amended. No new subject matter is added.

Claims 1-20 remain pending. Reconsideration of the pending claims is requested in light of the following remarks and arguments.

Amendments to the Drawings and Specification

The drawings were objected to for failing to show every feature of the invention specified in the claims.

With respect to color-coded markings (claims 3, 8, and 13), these are not shown in the drawings but they are nonetheless described adequately in the specification (page 6, lines 2-6).

With respect to demarcations (claim 7), claim 7 further specifies that the demarcations correspond to the location of chip boundaries. The applicants submit that demarcations corresponding to the location of chip boundaries are presently illustrated in the original drawings (FIG. 1).

With respect to markings having different shapes (claim 9), these are shown in the original drawings (FIG. 1), where it is seen that the markings 100 have different shapes. Markings of different shape are also amply described in the specification (page 6, lines 2-6). Nonetheless, the applicants agree that the markings 100 shown in FIG. 1 are small and have details that are difficult to discern.

With respect to the semiconductor defect inspection instrument (claim 10), it is not shown in the drawings but it is described as conventional art in the Description of the Related Art (page 1, lines 17-20). Claim 10 recites a wafer defect map where the location and type of wafer defects is determined using a semiconductor defect inspection instrument. Therefore, the semiconductor defect inspection instrument is a conventional feature disclosed in the description and claims, and because a detailed illustration of the semiconductor defect inspection instrument is not essential for a proper understanding of the invention, it should be illustrated in the drawing in the form of a graphical drawing symbol or a labeled representation (e.g., a labeled rectangular box) [37 C.F.R. 1.83(a)].

In keeping with the above comments, corrected drawings of FIG. 1 and FIG. 4A are submitted to overcome these objections. Corrected FIG. 1 has the content of original FIG. 1 plus the details of two individual marks having different colors and shapes. Corrected FIG.

4A has the content of original FIG. 1 plus an additional rectangular box that is labeled as a SEM (scanning electron microscope).

Appropriate amendments to the specification are also made to describe corrected FIGS. 1 and 4A.

Claim Rejections - 35 USC § 112

Claims 1-6, 8-9 and 13 stand rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding claim 1, it is amended to recite, in part, "marking defect locations on a wafer map using different types of marks to identify different types of defects." This amendment is fully supported by the specification at page 6, lines 2-6.

Regarding claim 2, it is amended to recite that different types of marks differ according to shape. This amendment is fully supported by the specification at page 6, line 6.

Regarding claim 3, it is amended to recite that different types of marks differ according to color. This amendment is fully supported by the specification at page 6, lines 3-6.

Regarding claims 4-6, the comments for claim 1 apply.

Regarding claim 8, it is amended to recite that each marking is configured to identify a type of defect by using a color that is associated with that type of defect. This amendment is fully supported by the specification at page 6, lines 3-6.

Regarding claim 9, as the Examiner notes, it is already fully supported by the specification (page 6, lines 2-6). No description of the different shapes used for each defect type is needed, because it is already evidently apparent to those of ordinary skill that a dot mark is just one example of a shape that might be used to indicate a type of defect. The claim is not intended to be limited to any particular shape or combination of shapes. Similarly, other claims are not intended to be limited to any particular color or combination of colors.

Regarding claim 13, it is amended to recite that preparing a wafer defect map to visually represent the location and type of the wafer defects comprises using marks on the wafer defect map that are assigned a color based upon the type of the wafer defect. This amendment is fully supported by the specification at page 6, lines 2-6.

The applicants submit that the rejections to claims 1-6, 8, 9, and 13 are overcome for the reasons outlined above.

Claim Rejections - 35 USC § 102

Claims 1-2, 4-7, 9-12, and 14-20 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,122,562 to Kinney et al. ('Kinney').

With regard to claim 1, it is amended to recite, in part, marking defect locations on a wafer map using different types of marks to identify different types of defects. This amendment is fully supported by the specification at page 6, lines 2-6.

Kinney does not contain the element of marking defect locations on a wafer map, rather Kinney marks defect locations on the surface of the wafer itself (column 2, line 4).

Kinney does not contain the element of using different types of marks to identify different types of defects, rather Kinney uses the same mark regardless of the type of defect. (column 2, lines 22-26).

The applicants submit that Kinney does not anticipate claims 1-2 and 4-6 for at least these reasons.

Further with respect to claim 2, it is amended to recite that different types of marks differ according to shape. This amendment is fully supported by the specification at page 6, line 6. Contrary to claim 2, Kinney uses the same shape of mark regardless of the type of defect (column 2, lines 22-26).

Further with respect to claim 4, Kinney does not disclose the claim limitation of graphing defect characteristics concurrently with marking defect locations on the wafer map. Kinney FIG. 5 shows a file structure 500 that is used to store the coordinate location of defects so that the file may be used in ***subsequent*** defect analysis stages such as SEM or AFM (column 7, lines 62-65, emphasis added). To the contrary, as explained in the specification (page 6, lines 7-11) "graphing defect characteristics" means arranging the characteristics of the defects into some sort of visual graph, such as the bar chart shown in FIG. 2. Thus, graphing defect characteristics occurs ***after*** defect analysis, not before the defects are analyzed as taught by Kinney. Furthermore, while the location of a defect might otherwise be considered a characteristic of the defect, it is clear from claim 4 that "graphing defect characteristics" and "marking defect locations" are different things. By storing coordinate locations of the defects in a defect file, all that Kinney FIG. 5 shows is another aspect of "marking defect locations."

Further with respect to claim 5, as explained previously in the comments for claim 4, while Kinney may disclose storing and analyzing defect ***locations***, Kinney does not teach storing and analyzing defect ***characteristics*** (column 4, lines 48-67, emphasis added).

Further with respect to claim 6, the applicants submit that Kinney FIG. 5 is not a graph that statistically analyzes the defects. Furthermore, the applicants submit that what Kinney teaches is a method of transforming defect locations in one coordinate system into defect locations in another coordinate system. Kinney does not teach using different marks on the wafer map to prepare graphs for statistical analysis of the defects (column 5, line 45 – column 6, line 23).

With regard to claim 7, it recites a wafer map comprising, in part, a schematic representation of a semiconductor wafer and a plurality of markings, where each marking is configured to identify a type of defect. As explained previously in the comments for claim 1, Kinney marks defect locations on the surface of the wafer itself (column 2, line 4), Kinney does not disclose a schematic representation of a semiconductor wafer. Additionally, similar to the comment for claim 1, Kinney does not disclose that each marking is configured to identify a type of defect. Rather, Kinney uses the same mark to identify the location of a defect, with no regard to the type of defect (column 2, lines 22-26).

The applicants submit that Kinney does not anticipate claims 7, 9, and 10 for at least these reasons.

Further with respect to claim 9, similar to the comment for claim 2, Kinney does not disclose that the markings have different shapes depending on the type of defect.

Regarding claim 11, it recites a method comprising, in part, preparing a wafer defect map to visually represent the location and type of each wafer defect and preparing one or more charts and/or graphs to statistically represent defect characteristics.

Similar to the comment for claim 1, Kinney does not disclose preparing a wafer defect map to visually represent the location and type of the wafer defects. Kinney marks defect locations on the surface of the wafer itself (column 2, line 4). Kinney uses the same mark regardless of the type of defect (column 2, lines 22-26).

Similar to the comment for claim 6, Kinney does not disclose preparing one or more charts or graphs to statistically represent defect characteristics. Kinney FIG. 5 is not a graph that statistically analyzes the defects, it is merely a file that stores defect locations.

The applicants submit that claims 11, 12, and 14-20 are not anticipated by Kinney for at least these reasons.

Further with regard to claim 12, similar to the comment for claim 1, Kinney does not disclose a wafer defect map.

With regard to claim 13, although it is initially indicated (Office Action, page 4, section 6) that claim 13 is not rejected under 35 U.S.C. § 102(b), an incomplete reference to

claim 13 appears on page 6 of the Office Action after the discussion of claim 12. The applicants assume that this particular reference to claim 13 was inadvertently left in the Office Action and will therefore not respond to it at this time.

Further with regard to claim 15, Kinney FIG. 5 shows an internal (not visible) file structure that is used to store the coordinate location of defects so that the file may be used in subsequent defect analysis stages such as SEM or AFM (column 7, lines 62-65). Consequently, Kinney does not disclose AES analysis.

Further with regard to claim 16, Kinney FIG. 5 shows only the location of defects, it does not show defect type, defect composition, and defect cause. Furthermore, similar to the comment for claim 4, Kinney FIG. 5 is a file structure, not a visible graph or chart.

Furthermore with regard to claim 17, nowhere does Kinney disclose preparing a bar graph representing the number of defects according to defect type.

Conclusion

For the foregoing reasons, reconsideration and allowance of claims 1-20 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

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Respectfully submitted,

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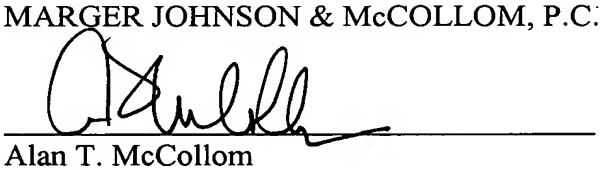

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